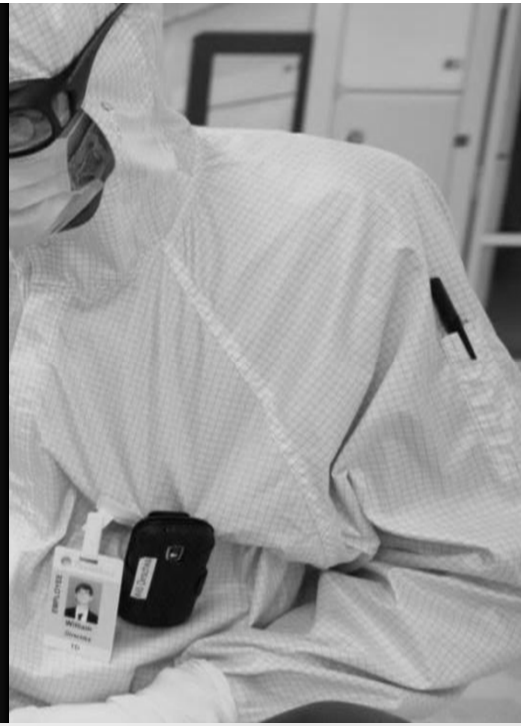

Effects of Phase Noise and Signal to Noise Ratio in PAM4 Signaling

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Introduction

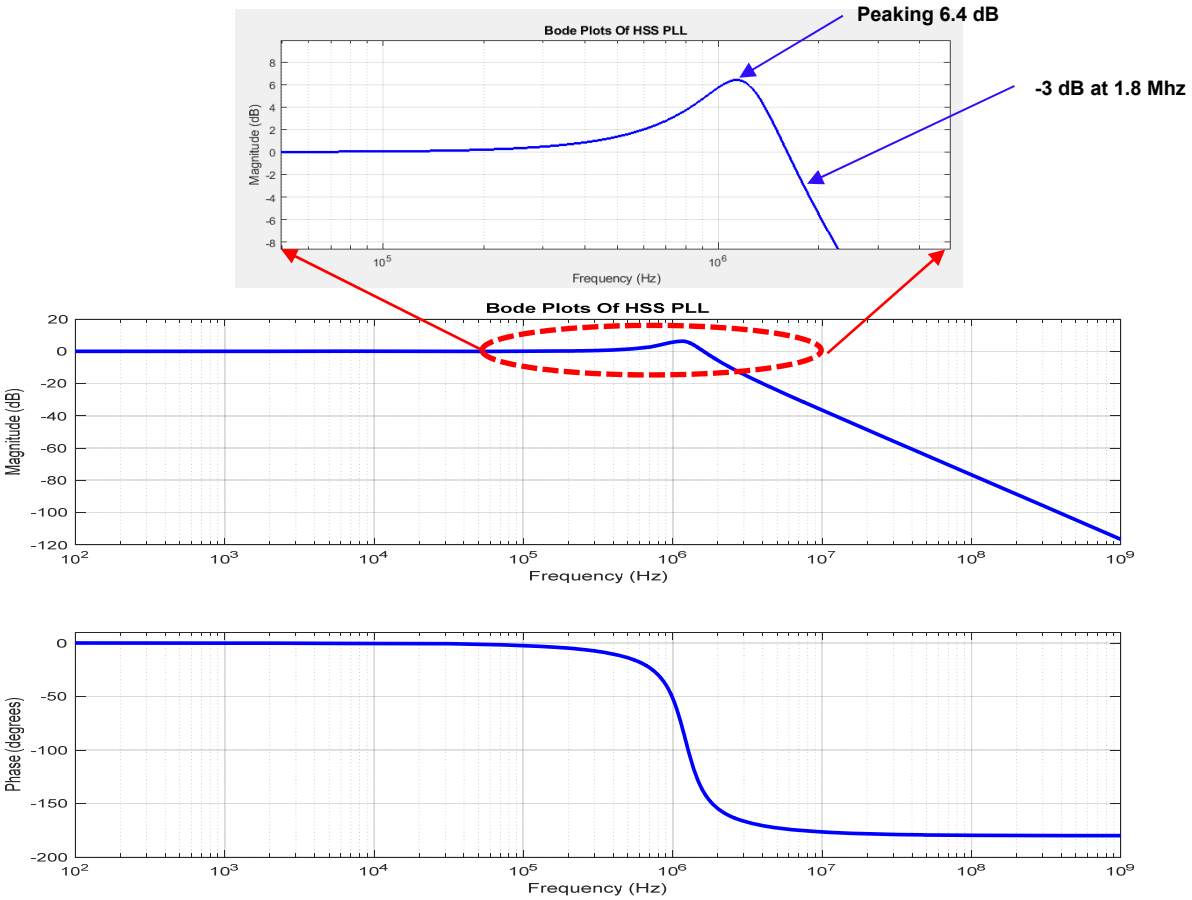
- Finding issues in a design is costly to schedule, and complex IPs such as HSS using PAM4 signaling are becoming more common on designs.

- Need a way to evaluate measured phase noise and/or channel signal to noise ratio and its effect on PAM4 signaling at the early stage of design engagement.

Agenda

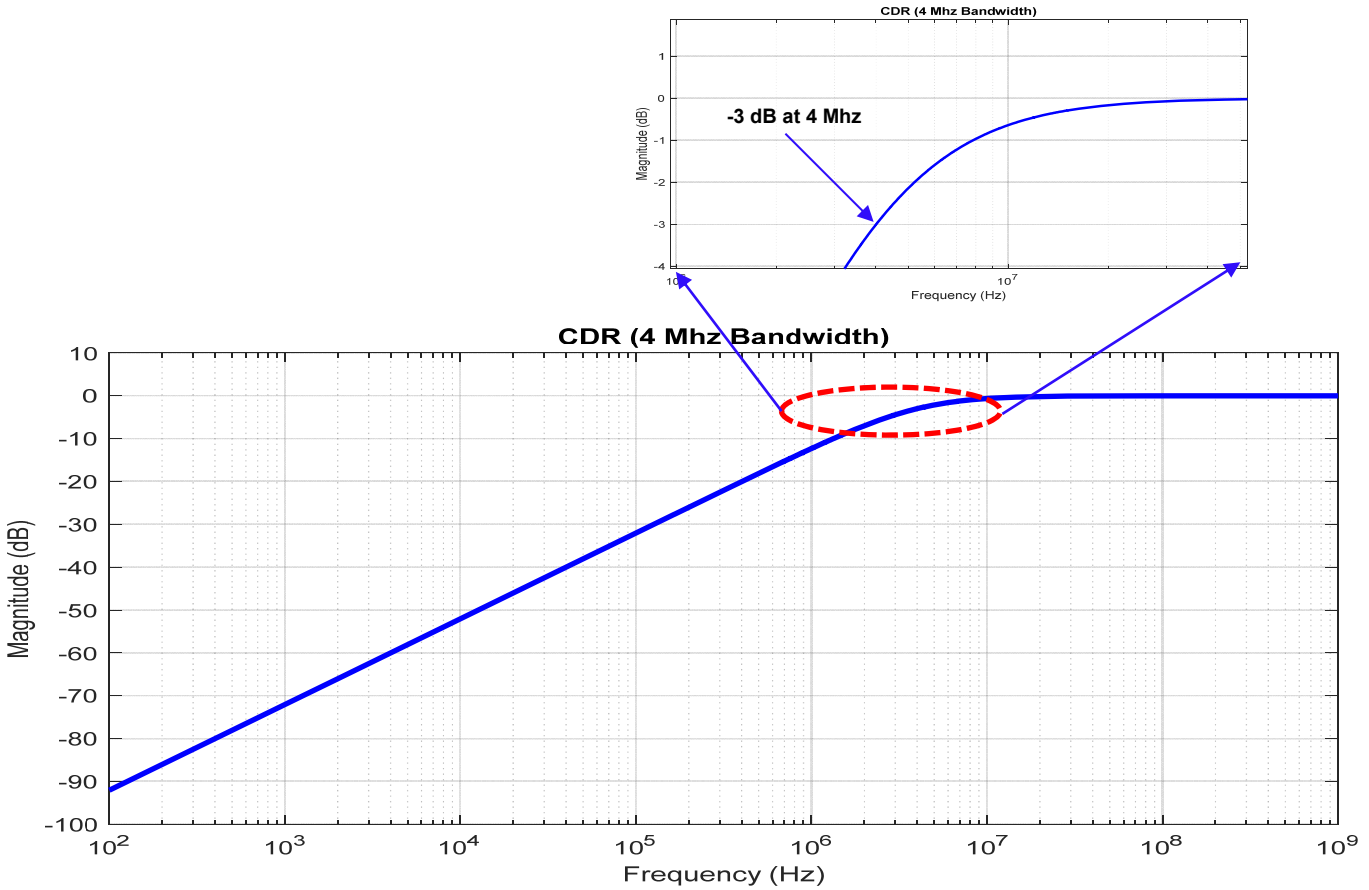
- Effect of Serial Link PLL and Clock Data Recovery (CDR).
- Overview of PAM4 signaling modeled to evaluate the effect of phase noise
- High level view of overall simulation setup. Modeled in using Matlab Simulink, Communication tool box, RF Tool Box and DSP toolbox.
- 5 different examples of “What if Scenarios” using phase noise and White Gaussian noise “Signal to Noise Ratio (SNR)”.

HSS PLL Model



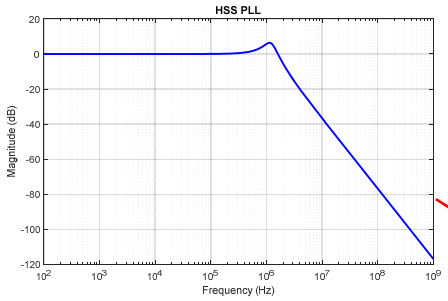
$$TF_{HSS\_PLL} = \frac{5.822e13}{s^2 + 3.766e6s + 5.822e13}$$

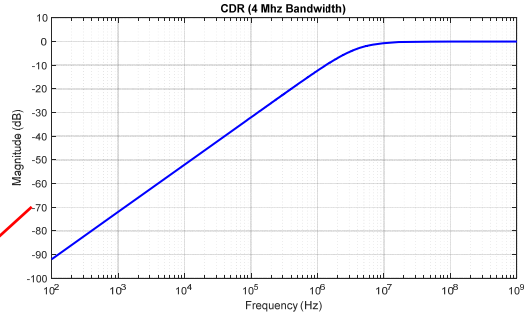
CDR Model

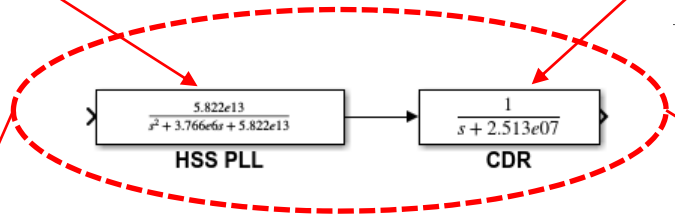


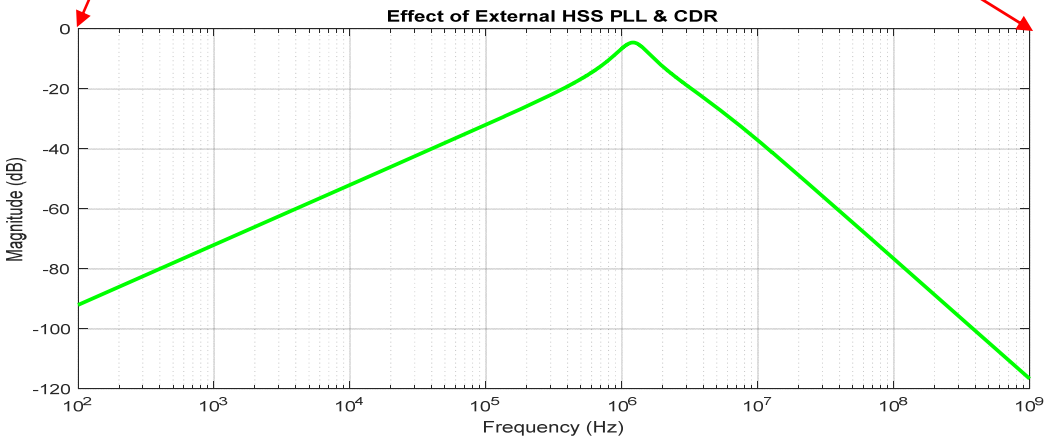
$$TF_{CDR} = \frac{s}{s + 2.513e7}$$

Effect of Tx PLL and CDR on phase noise



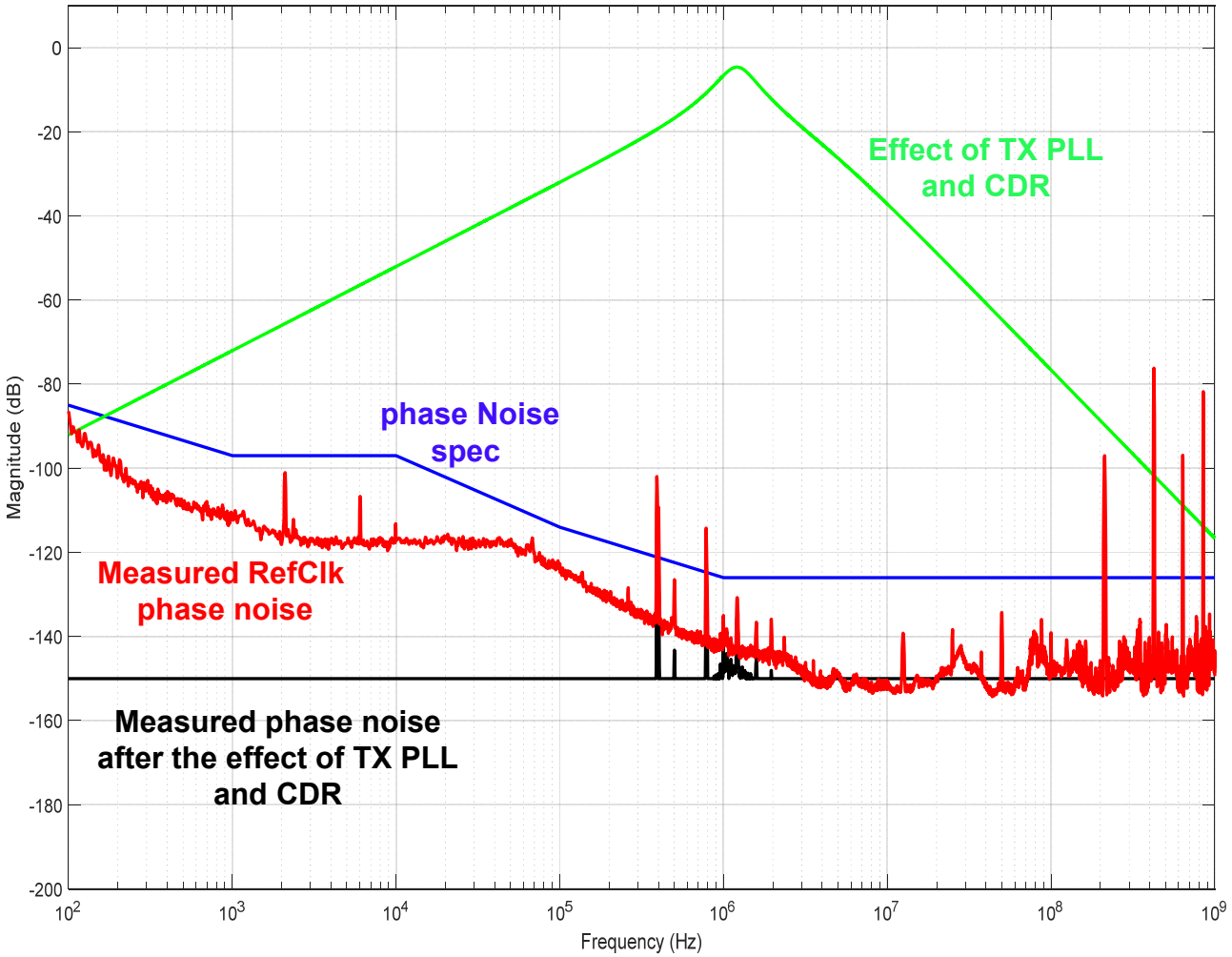




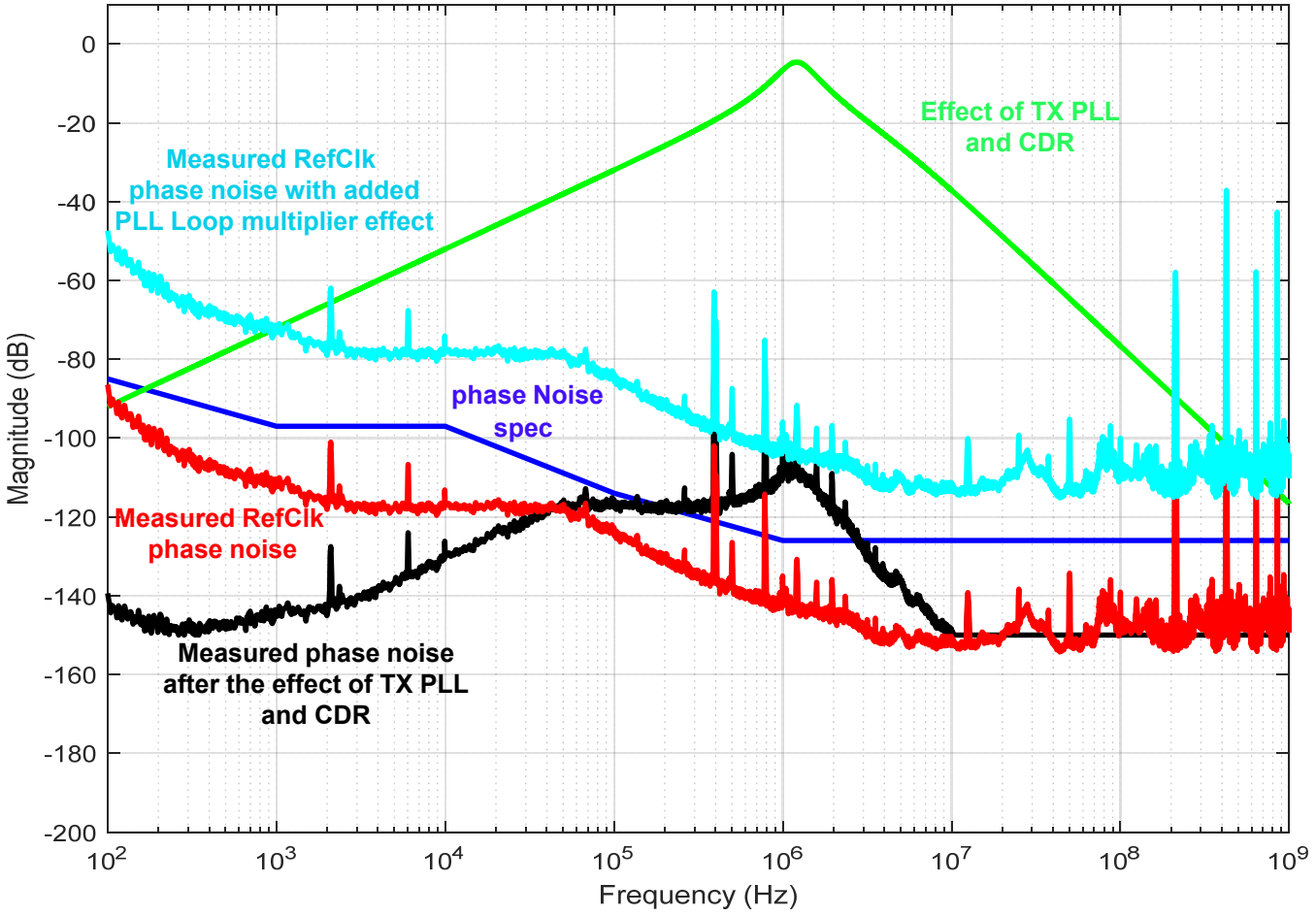


$$TF_{HSS\_PLL\&CDR} = \frac{5.822e13s}{s^3 + 2.89e7s^2 + 1.529e14s + 1.463e21}$$

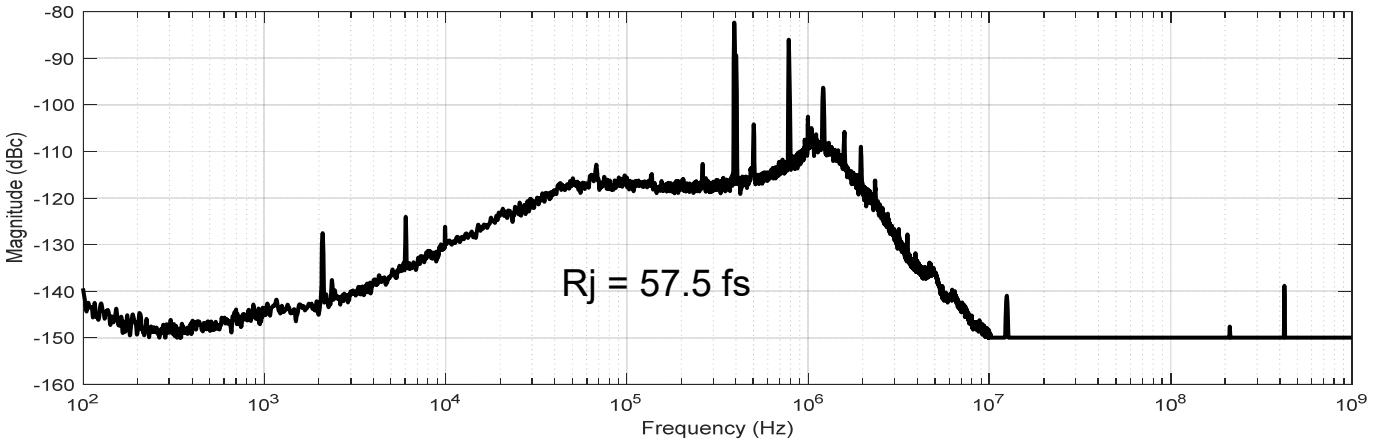
Effect of Tx PLL and CDR on phase noise continued….



Adding the effect of PLL loop multiplier to phase noise



Calculating Rj and Dj (Carrier = VCO = 14 Ghz)



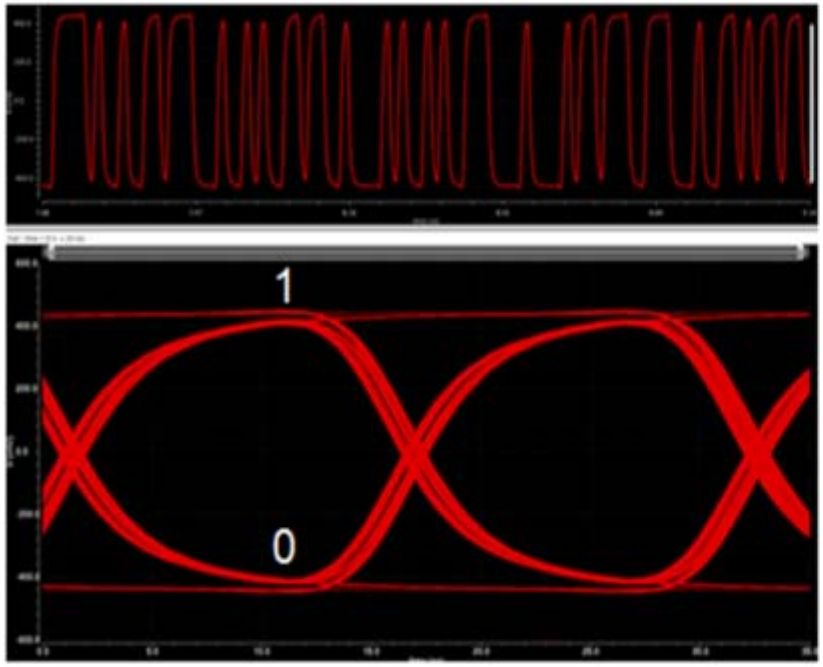
Freq(Hz)	dBc	Dj(sec)
2.1000e+03	-1.2750e+02	1.9176e-17
6.0300e+03	-1.2400e+02	2.8691e-17
3.9150e+05	-8.2280e+01	3.4975e-15
5.0100e+05	-1.0420e+02	2.8038e-16
7.8200e+05	-8.5960e+01	2.2896e-15
1.2120e+06	-9.6290e+01	6.9703e-16
1.5860e+06	-1.0580e+02	2.3321e-16
1.9530e+06	-1.0930e+02	1.5587e-16
1.2500e+07	-1.4100e+02	4.0528e-18
4.2500e+08	-1.3890e+02	5.1612e-18

Dominant Spur

Total Dj = $\sqrt{(1.9176e{-}17)^2 + \ldots\ldots\ldots\ldots + (5.1612e{-}18)^2} = 4.26\text{fs}$

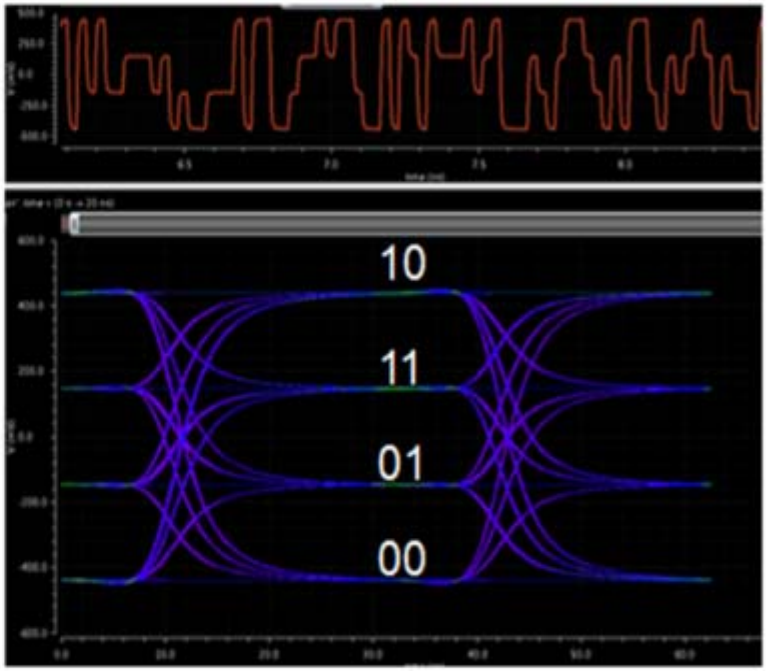
NRZ vs. PAM4 Signaling Examples

NRZ Signaling



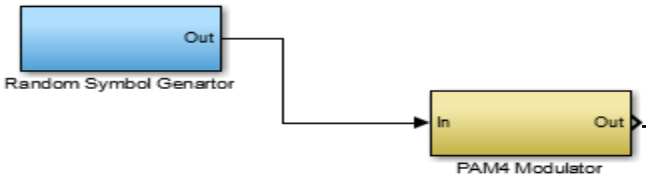
Two Levels: 0 / 1
1 bit per time period

PAM4 Signaling

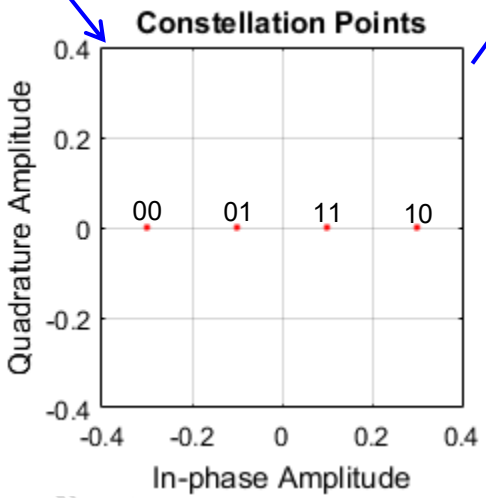


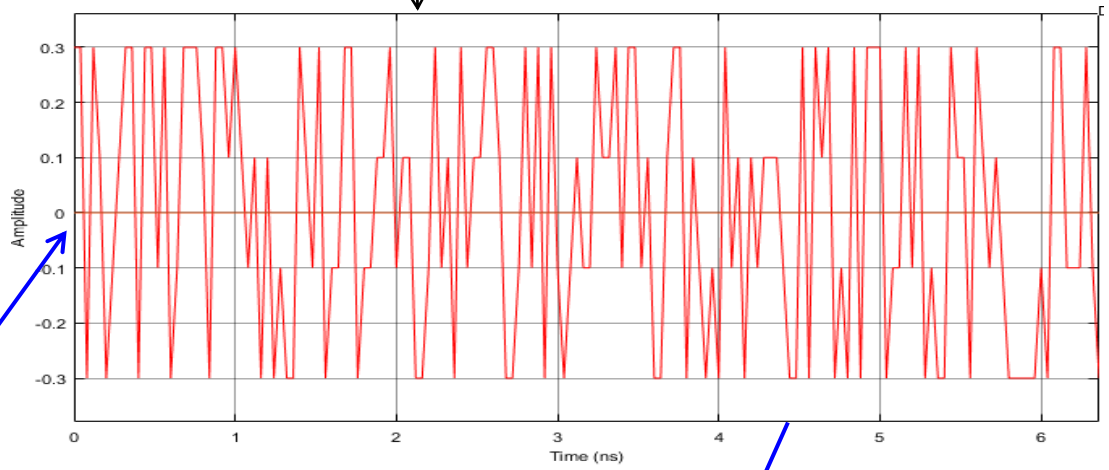
Four Levels: 00 , 01, 11, 10
2 bits per time period
(from perspective of input data)

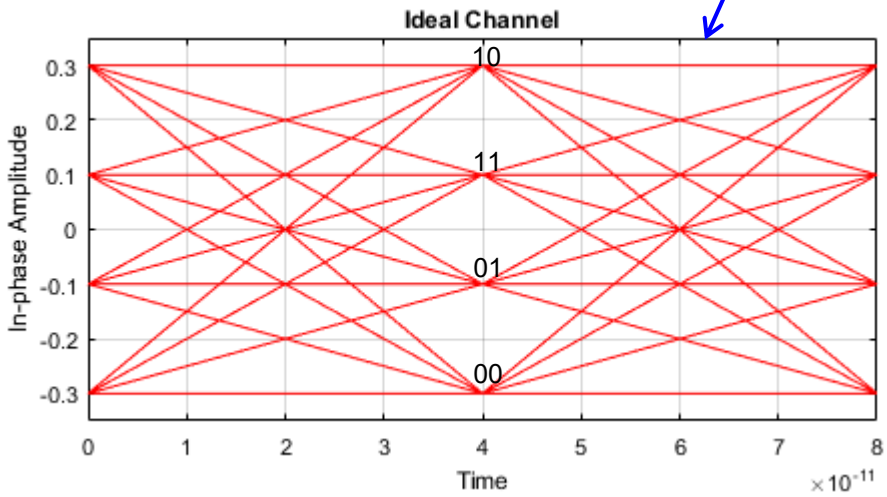
PAM4 Signaling



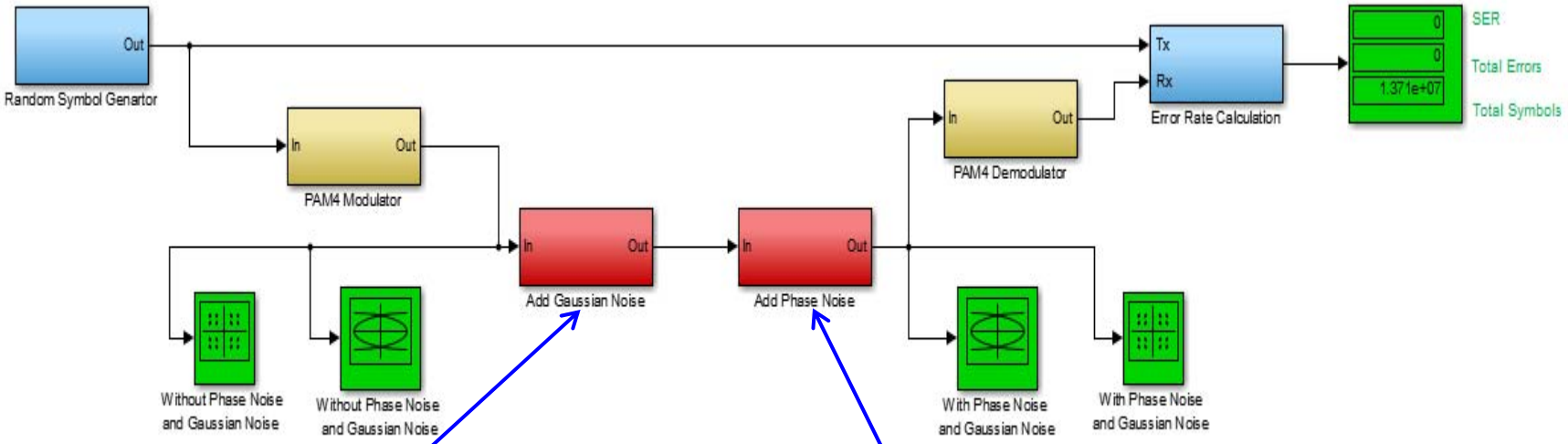
Adjusted PAM4 distance between two constellation points to produce amplitude of signal between 300mV to -300mV







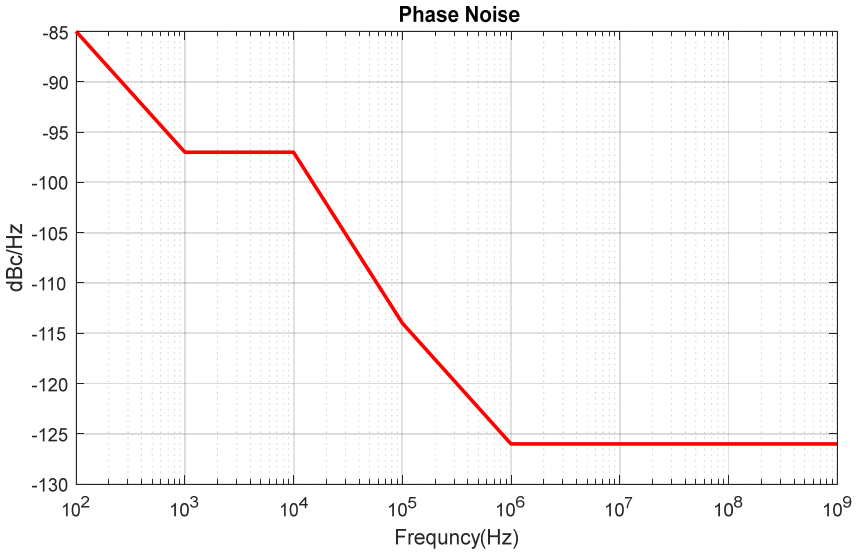
High level view of simulation setup



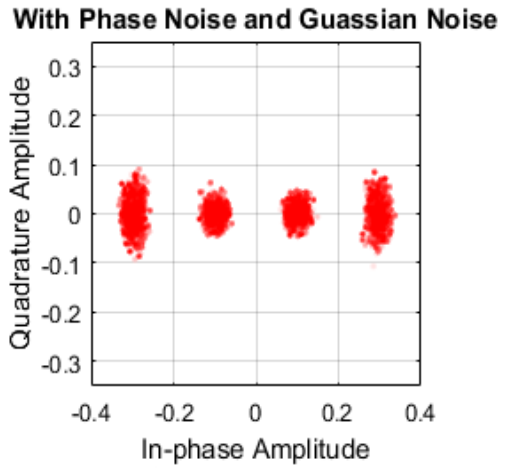
Add noise. Adds Gaussian white noise with user control signal to Noise ratio value.

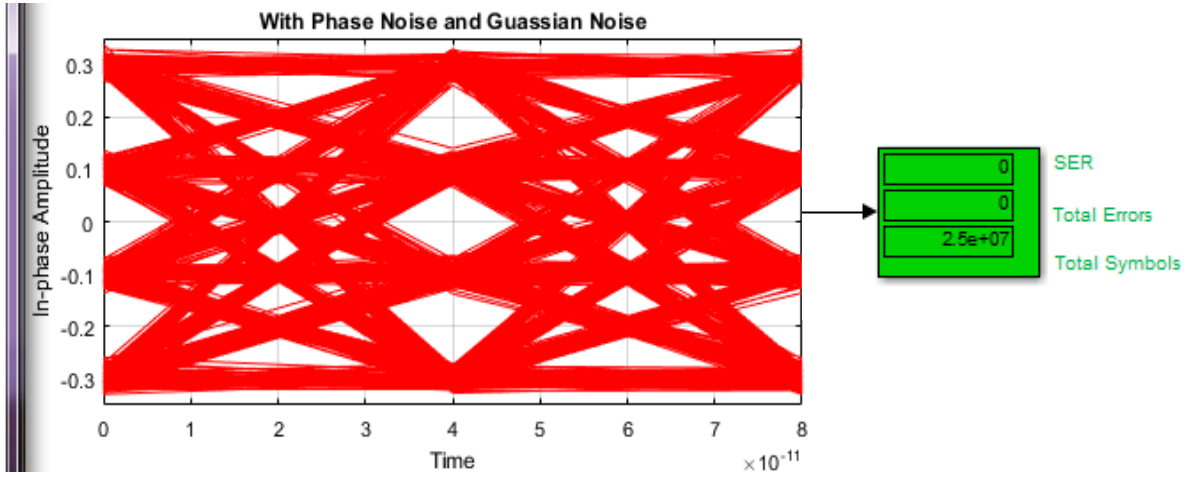
Read the entire phase noise data. Capability to evaluate the phase noise without spurs (Rj effect). Capability to evaluate effect of spurs and/or individual spur (Dj effect).

Simulation condition # 1

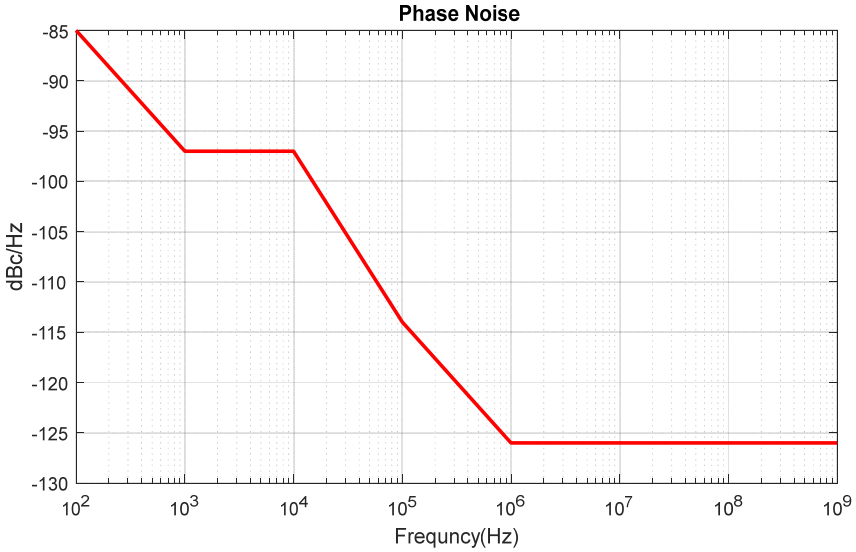


Signal to Noise Ratio = -35 dB

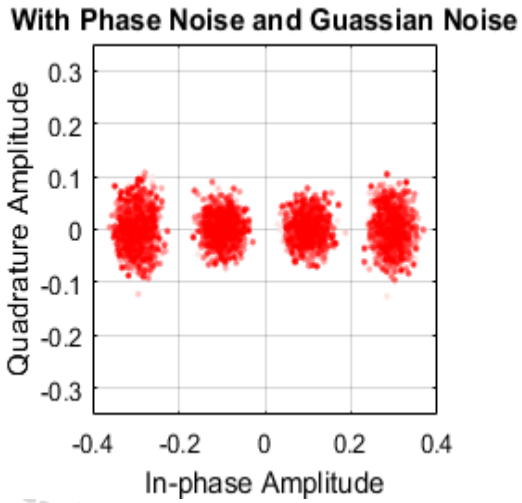


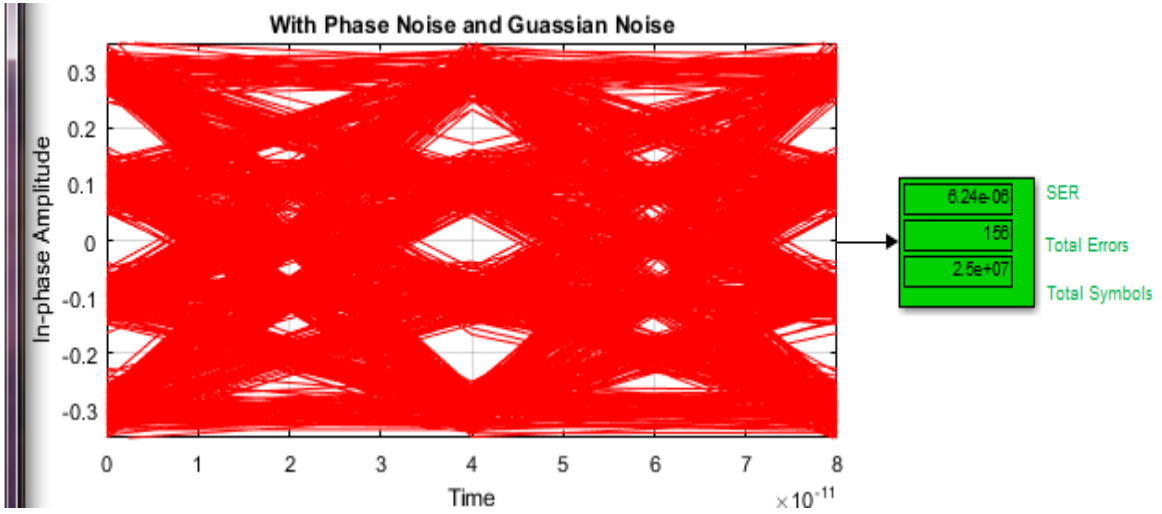


Simulation condition # 2

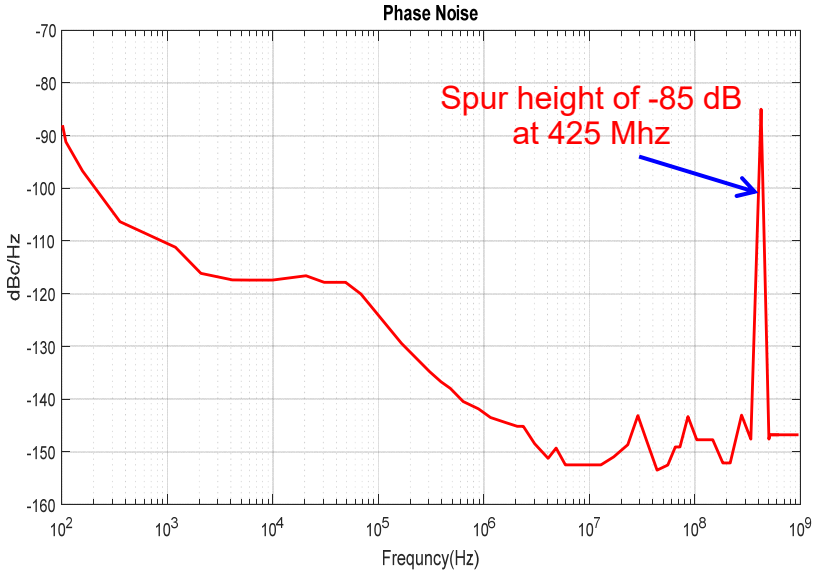


Signal to Noise Ratio = -30 dB

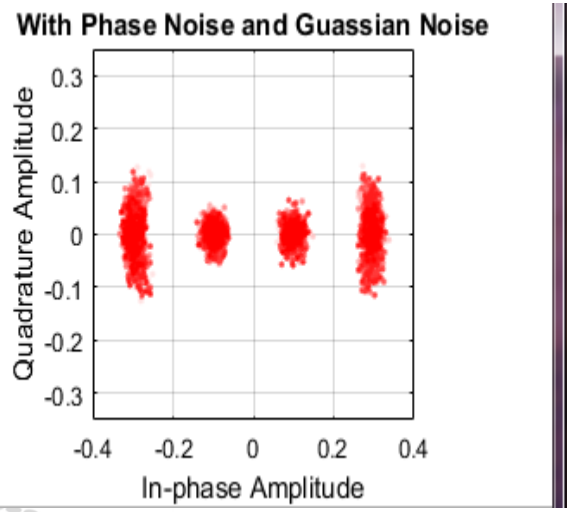


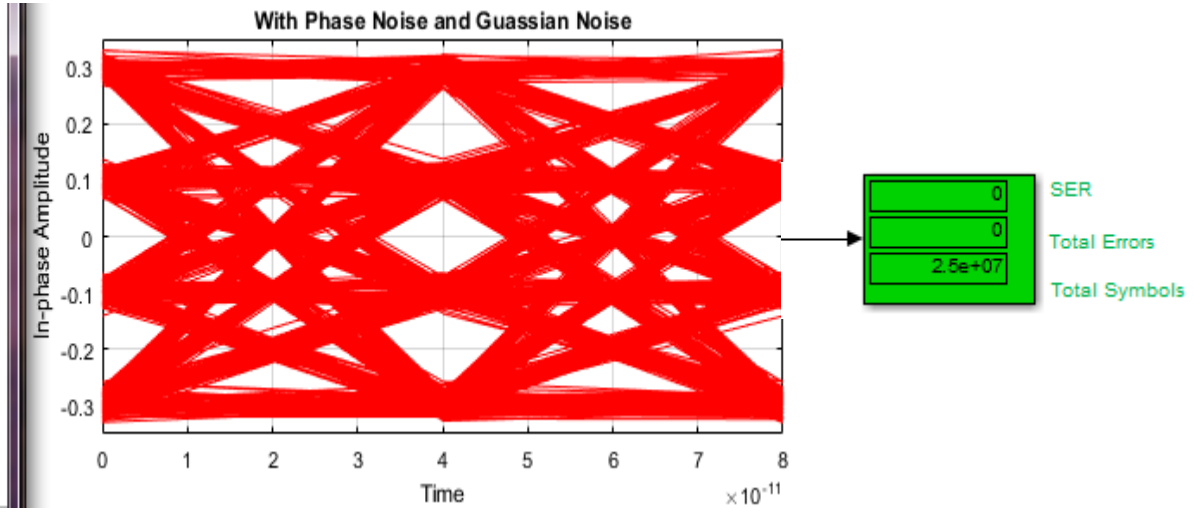


Simulation condition # 3

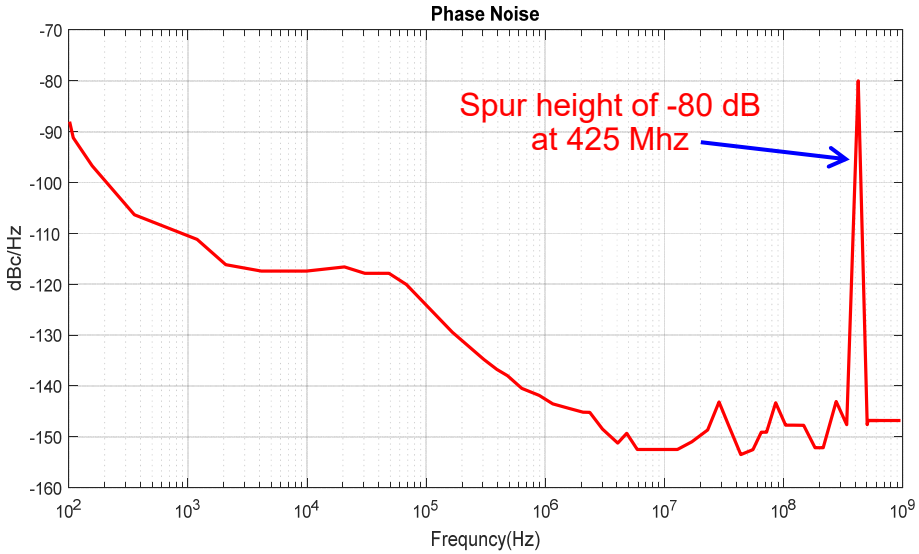


Signal to Noise Ratio = -35 dB

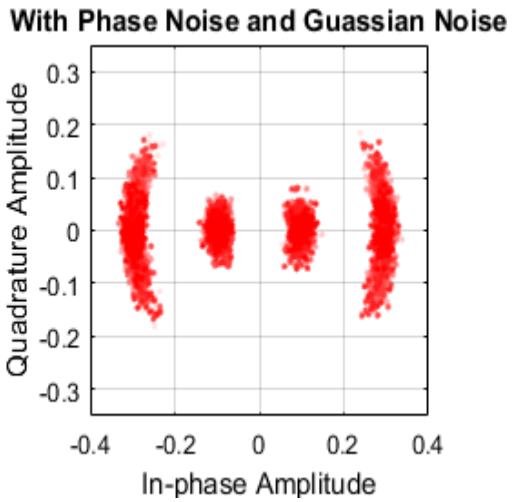


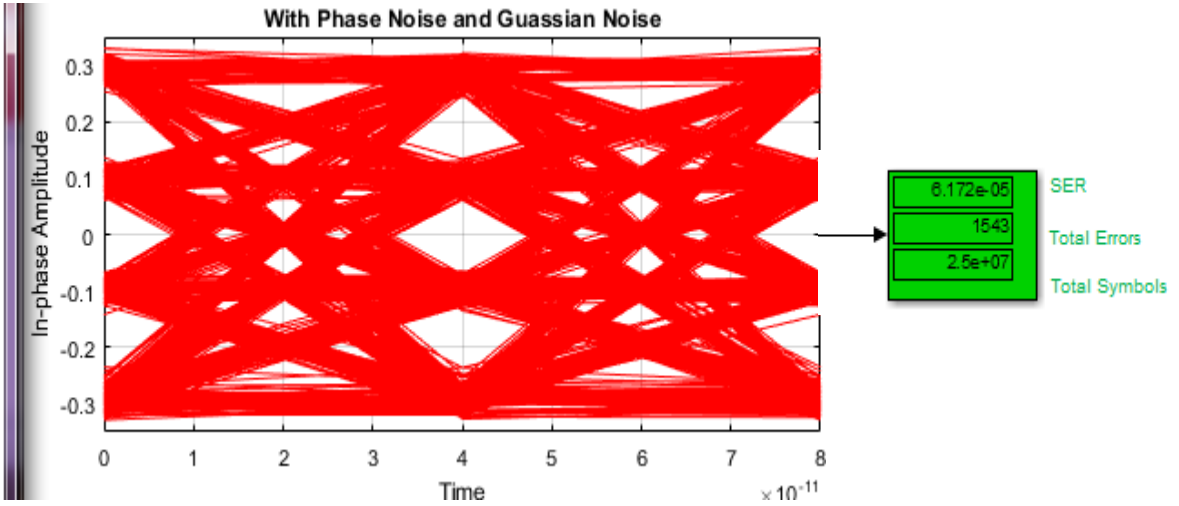


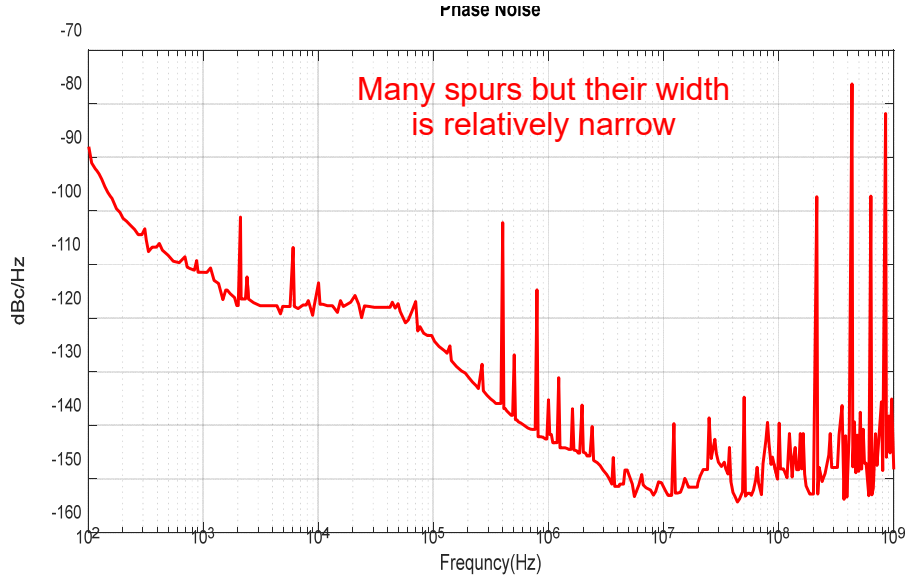
Simulation condition # 4



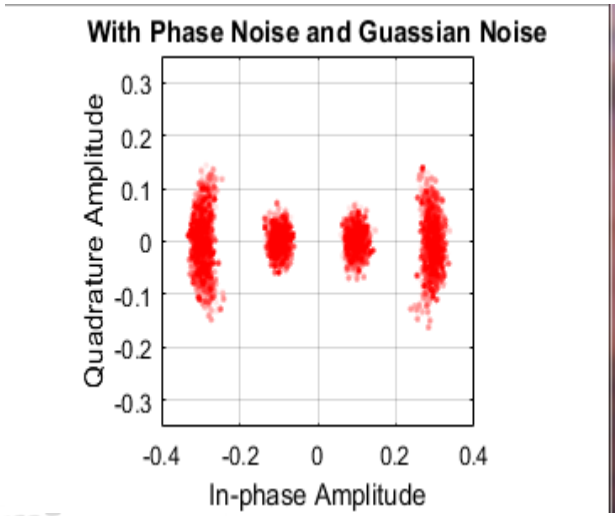
Signal to Noise Ratio = -35 dB

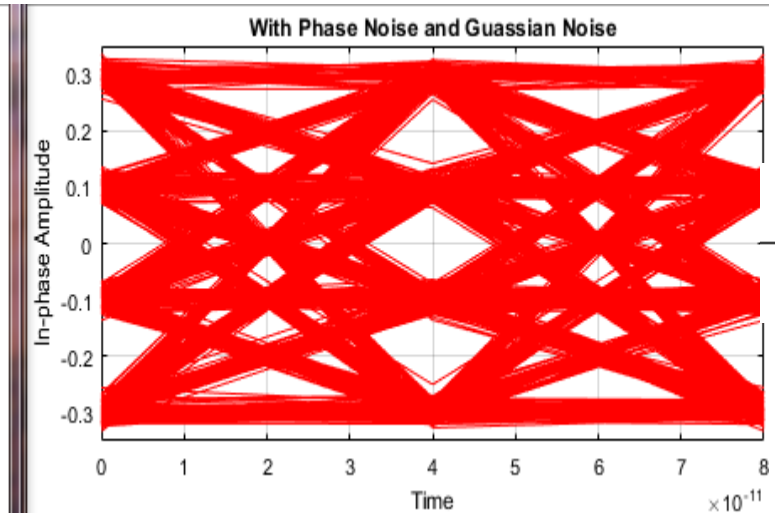


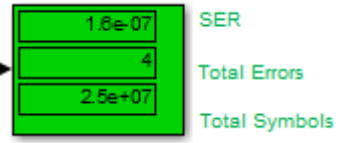




Signal to Noise Ratio = -35 dB







Summary

- The behavioral modeling of HSS PLL and CDR was demonstrated using Bode plots information and utilizing Matlab/Simulink Tool Boxes.
- Deterministic Jitter(Dj) was calculated based on the effect of HSS PLL closed loop Bandwidth, PLL loop multiplier and CDR using MJSQ guidelines.
- Tx and Rx are modeled as ideal without the effect of S-parameters and channel lost to isolate just the effect of carrier Phase Noise and “signal to noise” ratio of the system.
- The effect of phase noise in various scenarios were simulated. This includes evaluating phase noise without the spurs, with all the measured spurs and individual spur.
- The capability of detecting SER/Total Error based on the number of user defined symbol was demonstrated.

*MJSQ: *Methodologies for Jitter and Signal Quality Specification.*
*CDR: *Clock Data Recovery.*
*HSS: *High Speed Serial Link*
*Tx: *Transmitter.*
*RX: *Receiver.*
*SER: *Symbol Error Rate.*
*PAM4: *Pulse Amplitude Modulation.*
*VCO: *Voltage Controlled Oscillator.*
*Rj: *Random Jitter.*
*Dj: *Deterministic Jitter.*
*PLL: *Phase Locked Loop.*